Fabrication of graphene nanoribbon by local anodic oxidation lithography using atomic force microscope

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We conducted local anodic oxidation (LAO) lithography in single-layer, bilayer, and multilayer graphene using tapping-mode atomic force microscope. The width of insulating oxidized area depends systematically on the number of graphene layers. An 800-nm-wide bar-shaped device fabricated in single-layer graphene exhibits the half-integer quantum Hall effect. We also fabricated a 55-nm-wide graphene nanoribbon (GNR). The conductance of the GNR at the charge neutrality point was suppressed at low temperature, which suggests the opening of an energy gap due to lateral confinement of charge carriers. These results show that LAO lithography is an effective technique for the fabrication of graphene nanodevices.

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Graphene, a single atomic layer of graphite, has a unique band structure [1, 2] and exceptionally high carrier mobility [3]. Therefore, it has been used to develop carbon-based electronic devices [4]. To date, graphene nanodevices such as quantum dots [5, 6], Aharonov-Bohm rings [7], and nanoribbons [8, 9] have been fabricated by conventional electron-beam lithography combined with plasma etching. However, plasma etching introduces defects in graphene [3, 7, 10], which causes localization of charge carriers [7, 10]. Further, this technique cannot be used to control the edge structure of graphene, which is expected to have significant effects on its electronic properties [8]. Therefore, in order to fabricate high-quality devices, we need a new lithography technique that will allow us to perform high-resolution patterning without damaging the graphene layer.

Local anodic oxidation (LAO) lithography using atomic force microscope (AFM) is a promising technique for the fabrication of graphene nanodevices. This is because LAO lithography has been successfully used for fabricating nanodevices based on semiconductors [11, 12, 13, 14, 15]. The confinement of charge carriers obtained by LAO is highly specular [16] than that obtained by plasma etching [17], *i*.e. the charge carriers conserve their momentum along the normal to the confinement. Recently, Weng *et al.* produced insulating trenches in graphene flakes with a thickness of 1-2 atomic layers using tapping-mode AFM [18]. However, in their experiment, the number of graphene layers was not determined, though the LAO conditions such as the width of oxidized area are expected to be totally different for single-layer, bilayer, and multilayer graphene. Geisbers *et al.* used contact-mode AFM to produce an insulating trench on single-layer graphene [19]. However, the contact-mode AFM cantilever can damage the fabricated device [20]. Further, the transport phenomena of Dirac fermions were not demonstrated clearly in either experiment above [18, 19].

In this letter, we describe LAO lithography experiments that were conducted in single-layer, bilayer, and multilayer graphene using tapping-mode AFM. We show that the width of oxidized area depends on the number of graphene layers. We have fabricated an 800-nm-wide bar-shaped device, which exhibits the half-integer quantum Hall effect; this indicates that the conducting channel of graphene is intact during LAO. We have also fabricated a 55-nm-wide graphene nanoribbon (GNR). The conductance of the GNR at the charge neutrality point is strongly suppressed with decreasing temperature from $T = 300$ to 4.2 K. This suggests the opening of an energy gap due to the lateral confinement of charge carriers. These results show that LAO lithography is an effective technique for the fabrication of graphene nanodevices.

Graphene flakes were extracted from Kish graphite and deposited onto a 300-nm-thick SiO_2 layer by mechanical exfoliation [20]. Single-layer, bilayer, and multilayer graphene flakes were identified by the optical color contrast, and the number of graphene layers was verified by measuring the quantum Hall effect [1, 2] and Raman spectrum [21]. Two-terminal metal electrodes were fabricated by electron-beam lithography (Elionix ELS-7500) followed by thermal evaporation of Au/Cr (40/4 nm). Transport measurements were performed with the standard lock-in technique by applying a small AC current $I_{\rm AC} = 10$ nA (18 Hz). A heavily doped Si wafer was used as a global back gate to tune the carrier concentration. Before the transport measurements, surface impurities were removed by annealing the sample at $T = 420$ K in vacuum ($P \sim 1.0 \times 10^{-4}$ mbar) for several hours.

LAO lithography was performed in ambient air by tapping-mode AFM (JEOL JSPM-5200). The relative humidity was maintained at around 39−44%. The spring constant and resonance frequency of the conducting Si

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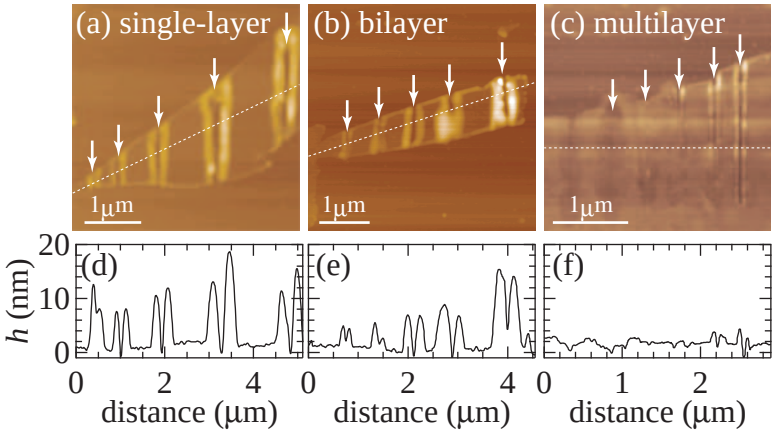

FIG. 1: (color online) AFM images of (a) single-layer, (b) bilayer, and (c) multilayer graphene. LAO nanolithography was carried out in the direction indicated by the white arrows at the scanning speeds of v_s = 160, 80, 40, 20, and 10 nm/s (left to right). (d), (e), and (f) show the cross-sectional height profiles along the white dashed lines in (a), (b), and (c), respectively.

cantilever were 42 N/m and 300 kHz, respectively. A positive DC bias voltage (35 V) was applied to the sample during the LAO lithography. The AFM cantilever was scanned with scanning speeds ranging from 10 to 160 nm/s.

Figure 1 shows AFM images of the (a) single-layer, (b) bilayer, and (c) multilayer graphene flakes. LAO lithography was performed by scanning the AFM cantilever in the directions indicated by white arrows at the scanning speeds of v_s = 160, 80, 40, 20, and 10 nm/s (left to right). The cross-sectional height profiles along the white dashed lines in Figs. 1(a)−(c) are shown in Figs. 1(d)−(f), respectively. When LAO lithography was performed in single-layer graphene, a narrow trench was fabricated, and a bump structure was formed on each side of the trench [Fig. 1(a)]. Trench and bump structures were also produced in bilayer graphene [Fig. 1(b)]. The previous studies on the fabrication of bump structures on HOPG (highly oriented pyrolytic graphite) and graphene [18] did not determine the electronic properties of the bump region. In order to investigate the conductance of the bump regions, we fabricated a device in which carrier transport can occur through a 100-nm-wide and 800-nm-long bump region (not shown). The two-terminal resistance of the device at room temperature was greater than 1 GΩ independent of the gate bias voltage. This implies that the bump region is an insulating region, which may consist of nonvolatile graphene oxide. Therefore, the effective width of the insulating region w can be obtained by adding the widths of the trench and bump regions.

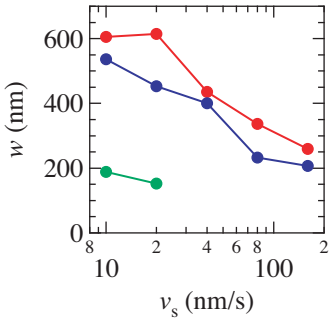

FIG. 2: (color online) (a) Width of the insulating region w formed in single-layer (red), bilayer (blue), and multilayer (green) graphene as a function of the scanning speed of the AFM cantilever v_s.

Figure 2(a) shows w as a function of v_s for single-layer, bilayer, and multilayer graphene. The value of w decreases with v_s. This implies that the resolution of LAO lithography increases with v_s. Also, w significantly decreases with the number of graphene layers. This suggests that the robustness of graphene flakes against LAO increases with the number of graphene layers.

To investigate the influence of LAO lithography on the electric properties of graphene, we fabricated an 800-nm-wide bar-shaped device as shown in Fig. 3(a). The two-terminal conductance G [22] decreases sharply at V_g = 5 V [Fig. 3(b)]. This shows that the charge neutrality point of this device is placed close to zero $V_{Dirac} \sim 5$ V. The result obtained here is in sharp contrast to that obtained in a device covered with a protective mask of hydrogen silsesquioxane (HSQ) for oxygen plasma etching, where a large positive shift of $V_{Dirac} > 50$ V was induced by the presence of HSQ layer even after the annealing process in vacuum [9]. The electron mobility of the graphene layer is $\mu \sim 7000$ cm^2/Vs at V_g = 25 V, which is comparable to μ of our single-layer graphene devices measured before LAO lithography. This indicates that the conducting channel of graphene is intact during LAO lithography. Figure 3(c) shows G as a function of V_g measured at T = 4.2 K in a magnetic field of B = 9 T. We can clearly observe the quantum Hall plateaus at $G = 2, 6, 10$, and 14 e^2/h and V_g = 12, 22, 35, and 45 V, respectively. The quantized plateaus in the sequence $G = 4(N + 1/2)$ (e^2/h), where N is an integer, are indica-

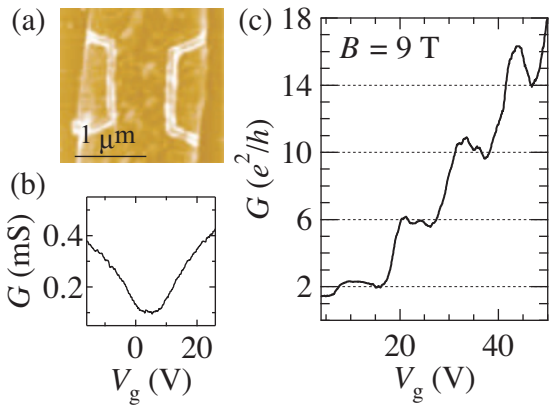

FIG. 3: (color online) (a) AFM image of the bar-shaped device fabricated in single-layer graphene. (b) Two-terminal conductance G as a function of the gate-bias voltage $V_{\rm g}$ measured at $T = 4.2$ K in a zero magnetic field. (c) G as a function of $V_{\rm g}$ measured at $T = 4.2$ K and $B = 9$ T.

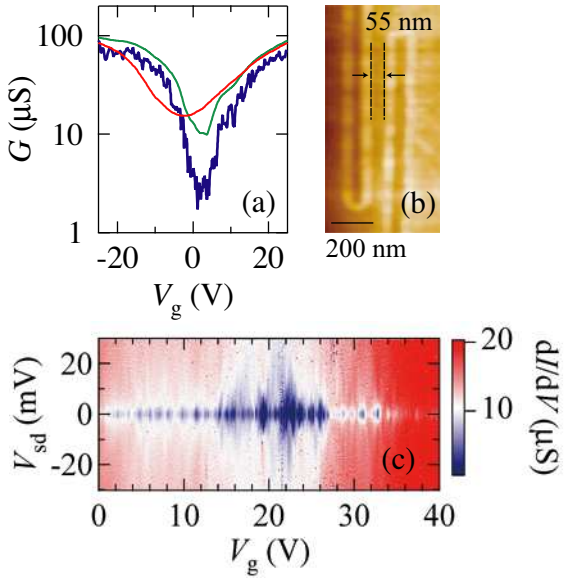

FIG. 4: (color online) (a) Two-terminal conductance G of the device mentioned in (b) as a function of the gate-bias voltage $V_{\rm g}$ measured at $T = 300$ (red), 77 (green), and 4.2 K (blue) in a zero magnetic field. (b) AFM image of a 55-nm-wide (W) and 800-nm-long (L) nanoribbon formed in single-layer graphene. (c) Color plot of the differential conductance $\mathrm{d}I/\mathrm{d}V$ of the 77-nm-wide and 600-nm-long nanoribbon as a function of the gate-bias voltage $V_{\rm g}$ and the source-drain bias voltage $V_{\rm sd}$.

tive of the half-integer quantum Hall effect. Thus, this result shows that LAO lithography is an efficient technique for the fabrication of graphene devices that exhibit the characteristics of Dirac fermions.

Finally, we studied the transport properties of graphene nanoribbons (GNRs) whose widths were $W =$ 55 [Fig. 4(b)] and 77 nm (not shown). Each GNR was connected to the metal electrodes through the 2-μm-wide graphene blocks. Thus, G is restricted by the GNR region. Figure 4(a) shows G of the GNR with $W = 55$ nm as a function of $V_{\rm g}$ measured at $T = 300$ (red), 77 (green), and 4.2 K (blue). At $T = 300$ K, G is minimum at $G_{\rm min} \sim 4e^2/h\ (W/L)$. When the temperature is decreased to $T =$ 4.2 K, $G_{\rm min}$ is suppressed by ten times [blue curve in Fig. 4(b)]. The suppression of $G_{\rm min}$ at low temperature is in sharp contrast to the result that $G_{\rm min}$ reduces only by 5% from $T = 300$ to 4.2 K in the single-layer graphene before LAO (not shown). Figure 4(c) shows the color plot of the differential conductance $\mathrm{d}I/\mathrm{d}V$ of the GNR with $W = 77$ nm as a function of $V_{\rm g}$ and source-drain bias voltage $V_{\rm sd}$. In Fig. 4(c), the region of suppressed conductance (dark area) forms diamond-like pattern at around the charge neutrality point. The results presented in Figs. 4(a) and 4(c) quantitatively agree with those observed in GNRs fabricated by oxygen plasma etching [8, 23]. Thus, our results suggest the opening of an energy gap $E_{\rm g}$ due to the lateral confinement of charge carriers. Further, the value of $V_{\rm sd}$ at the vertex of the dark area gives an energy gap $E_{\rm g} \sim 5$ meV [Fig. 4(c)]. This is quantitatively comparable to that obtained in the 60-nm-wide GNR fabricated by the oxygen plasma etching [8].

In summary, we have conducted LAO lithography in single-layer, bilayer, and multilayer graphene using AFM. We showed that the width of the oxidized area depends on the number of graphene layers. We fabricated an 800-nm-wide bar-shaped device, which exhibits the half-integer quantum Hall effect. We also fabricated a 55-nm-wide graphene nanoribbon (GNR). The conductance of the GNR at the charge neutrality point was strongly suppressed by decreasing T. These results show that LAO lithography is an effective technique for the fabrication of graphene nanodevices.

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